Proc. Annual Symposium on Research & Industrial Training, 01(2014) 11-14
Department of Electronics – Wayamba University of Sri Lanka

STUDY OF IMAGE PROCESSING ALGORITHMS FOR HARDWARE IMPLEMENTATION

B. G. Jayakody*,W. A. S. Wijesinghe,

Department of Electronics Wayamba University of Sri Lanka, Kuliyapitiya, Sri Lanka.
*buddhimagayan@gmail.com**

ABSTRACT

The study presents a hardware implementation of real time Image processing algorithm. Image processing algorithms are usually implemented in software. There is an increasing demand for real-time image processing in applications such as industrial automation and robotics. Software implementations of image processing algorithms are not suitable for real-time applications due to slower processing power. In this study we propose hardware implementation of image contrast enhancement using a Field Programmable Gate Array (FPGA). The results of the study show that a large speed performance can be achieved by hardware implementation than the software implementation.

Key words: *FPGA, HDL, Contrast Enhancement*

1.0 INTRODUCTION

In past decade, image processing has huge improvement and it used for lot of industrial application. But most of image processing application has made using software implementation methods. Software implemented applications consume much considerable time to perform their process[1].So software implementation could not use for the real time application. Hardware implementation is solution for that delay of the software implemented application. FPGA is the one of latest popular hardware device which used for the image processing real time application.

Image processing hardware implementation is used for many applications in modern world. Medicine, space exploration, surveillance, authentication, automated industry inspection and many more areas used hardware implementation application of image processing for real time operation[2].

Contrast enhancement techniques are used to improve the visibility of the image without unrealistic color effect.

Most of the image contrast-enhancement techniquesare applied to grayscale images. However, the evolution of photography has increased the interest in color imaging and consequently in color contrast-enhancementmethods[3].

2.0 EXPERIMENTAL

In past few years FPGA became more popular among researchers who do the experiments using hardware implementation devices. More recently, FPGAs such as a Xilinx has come to rival corresponding ASIC and ASSP solutions by providing significantly reduced power, increased speed, lower materials cost, minimal implementation real-estate, and increased possibilities for re-configuration 'on-the-fly'.Where previously a design may have included 6 to 10 ASICs, the same design can now be achieved using only one FPGA[4].Xilinx sparten 3E development Board is used for that project.

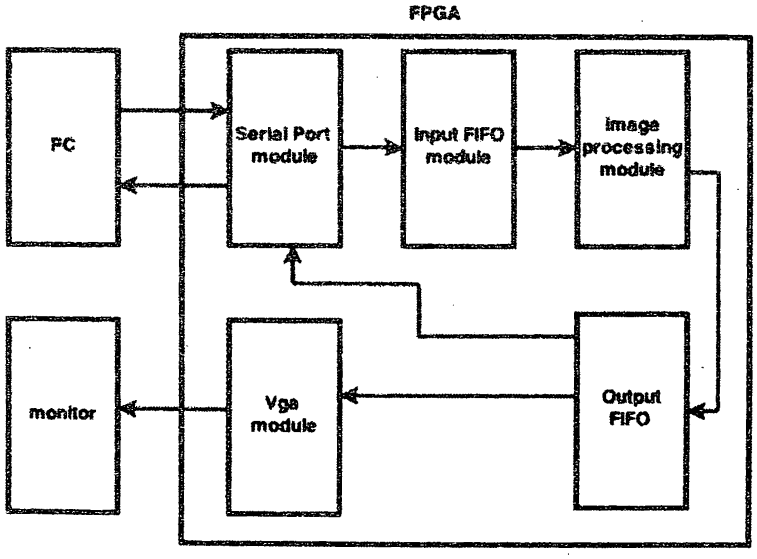

Figure 1: Block Diagram of the Image Processing System (IPS)

Original image exist in the computer and digital information of the image transfer to FPGA board through communication link. Serial communication is used as a communication link. Then FPGA board perform some operation to that digital data for enhance the contrast of the image. After the process, new image display through VGA output. First In, First Out

(FIFO), a method for organizing and manipulating a data buffer that control the flow of the data.

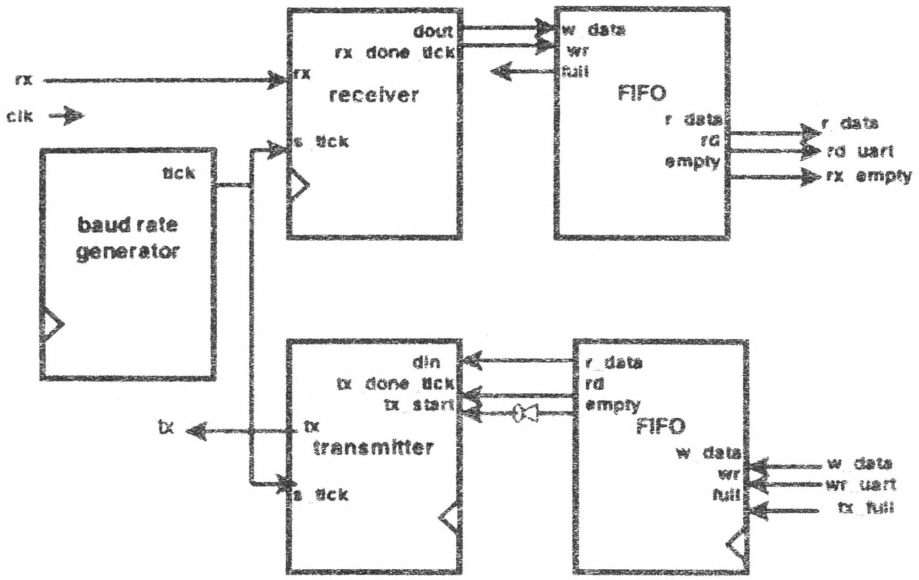

Figure 2: Block Diagram of the Serial Communication Link

3.0 RESULTS AND DISCUSSION

Figure 3 presents Isim simulation related to theinput digital information of the image and output dataafter the process.

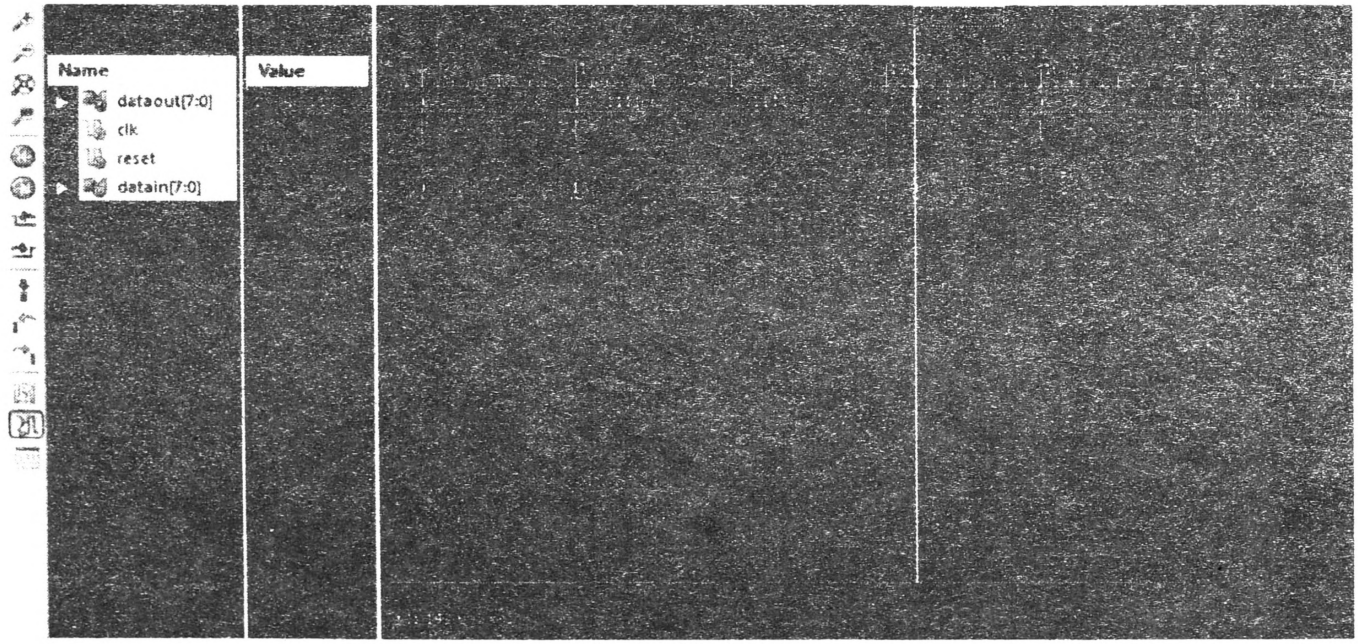

Figure 3: simulation results with Isim tool

Field-programmable gate arrays (FPGAs) are non-conventional processors built primarily out of logic blocks connected by programmable wires. Each logic block has one or more lookup tables (LUTs) and several bits of memory[5]. As a result, logic blocks can implement arbitrary logic functions (up to a few bits). Logic blocks can be connected into circuits of arbitrary complexity by using the programmable wires to route the outputs of logic blocks to the input of others. FPGAs as a whole can therefore implement circuit diagrams, by mapping the gates and registers onto logic blocks.

All FPGAs have special purpose I/O blocks that communicate with external pins. Many have on-chip memory in the form of RAM blocks. Others have multipliers or even complete RISC processors in addition to general purpose logic blocks[5].

4.0 CONCLUSION

The industrial applications and robotics require real-time image processing methods. Software implementations of image processing algorithms do not suitable for real-time applications due to slower speed performance. In this study we attempted to implement contrast enhancement algorithm on a Xilinx SpartanFPGA. Results show that the hardware implementation of the algorithm is about ten times faster than the software implementation of the same algorithm.

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