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FPGA BASED CAMERA INTERFACE FOR REAL TIME VIDEO PROCESSING

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ABSTRACT

This paper describes the design and implementation of a camera interface on a Field Programmable Gate Array (FPGA). An FPGA contains configurable logic resources, which can be used to implement algorithms in hardware for speed performance than software implementations. Real-time video processing is a field that demands higher processing power, and FPGAs are ideal candidates for video processing applications. However, most cameras come with software drivers, which are not suitable for high performance video processing in FPGAs. In this study we present a hardware camera interface for a cheap camera module (OV7670) using an Altera Cyclone IV FPGA (EP4CE15). The designed system captures continuous video streams from the camera module and displays on the VGA display. The system uses about 3% of total logic elements of the FPGA. The rest of the logic resources can be used to implement different functions in hardware for real-time video processing.

Keywords: FPGA, OV7670, NIOS, CYCLONE

1. INTRODUCTION

Real-time video and image processing is used in a wide variety of applications from video surveillanceand traffic management to medical imaging applications. These operations typically require very high computation power. Standard definition NTSC video is digitized at 720x480 or full D1 resolution at 30frames per second, which results in a 31MHz pixelrate. With multiple adaptive convolution stages todetect or eliminate different features within the image, the filtering operation receives input data at a rate ofover 1 Giga samples per second. Coupled with newhigh-resolution standards and multi-channelenvironments, processing requirements can be evenhigher. Achieving this level of processing power requires multiple

processors. Asingle FPGA with an embedded soft processor candeliver the requisite level of computing power morecost-effectively, while simplifying board complexity.[1]

And the other hand video processing using software platforms is very time consuming and the Hardware for the computers must be in high level.In this project a hardware interface for camera module was developed. The implementation was based around a small camera module using on the OmniVision 7670 CMOS VGA CameraChip, OV7670. The OV7670 is a low voltage CMOS image sensor that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7670 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface. This product has an image array capable of operating at up to 30 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, Omni Visioncamera chip use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise (FPN), smearing, blooming, etc., to produce a clean, fully stable color image.

A custom Altera FPGA NIOS CYCLONE IV EP4CE15 development board was used for the development of hardware interface. The Altera development board is based on NIOS Cyclone IV EP4CE15F17C8N FPGA chip. The development board is equipment with SDRAM 256Mbit (16M*16bit), SRAM: 4Mbit (256K*16bit), Serial FLASH: 64Mbit (EPCS64), Parallel FLASH: 32Mbit (4M*8bit), Crystal: 50MHZ and 40MHZ, 110 of I/O and AS and JTAGas download debug port.

This paper presents the implementation of hardware interface between OV7670 camera module and a VGA monitor for real time video processing.

2. EXPERIMENTALMETHODOLOGY

The OV7670 camera module is a low voltage CMOS image sensor that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7670 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface. This product

has an image array capable of operating at up to 30 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer.

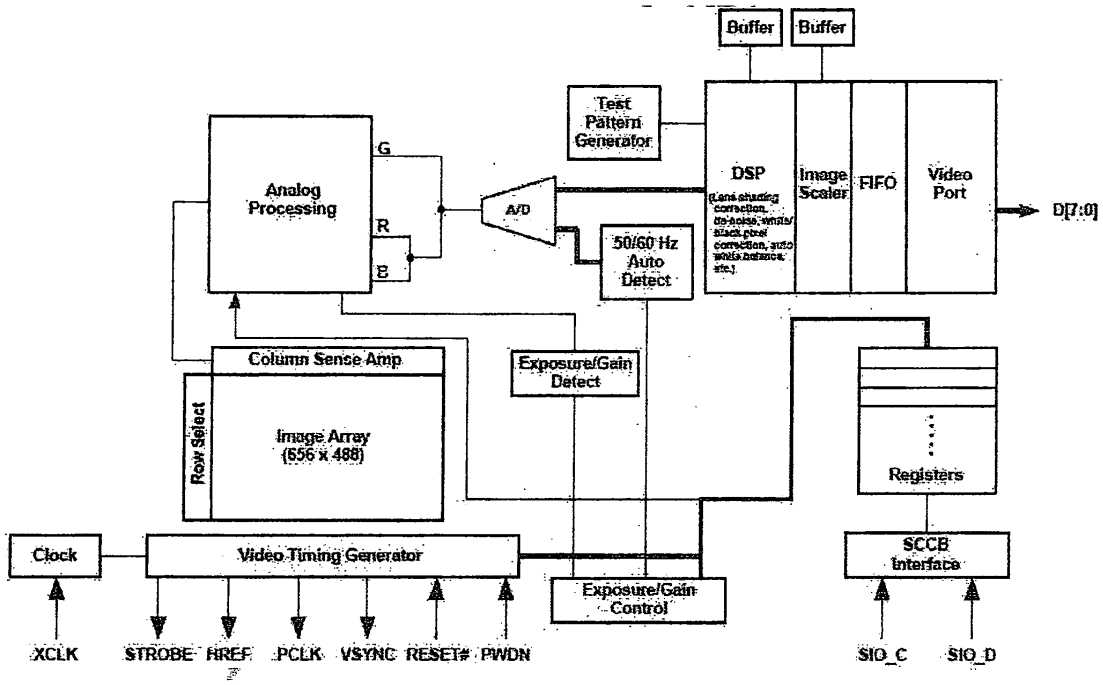

Figure 1: Functional Block Diagram of OV7670

The camera is interfaced with the FPGA board for which the controller module and capture logic module have developed as shown in Figure 2. With the help of controller module and capture logic module the camera is interfaced with the FPGA board for data capturing and streaming it in the display unit. Frame Buffer storing the pixel information in the Simple Dual Port RAM of FPGA and streaming them to the VGA monitor as 12bit output.

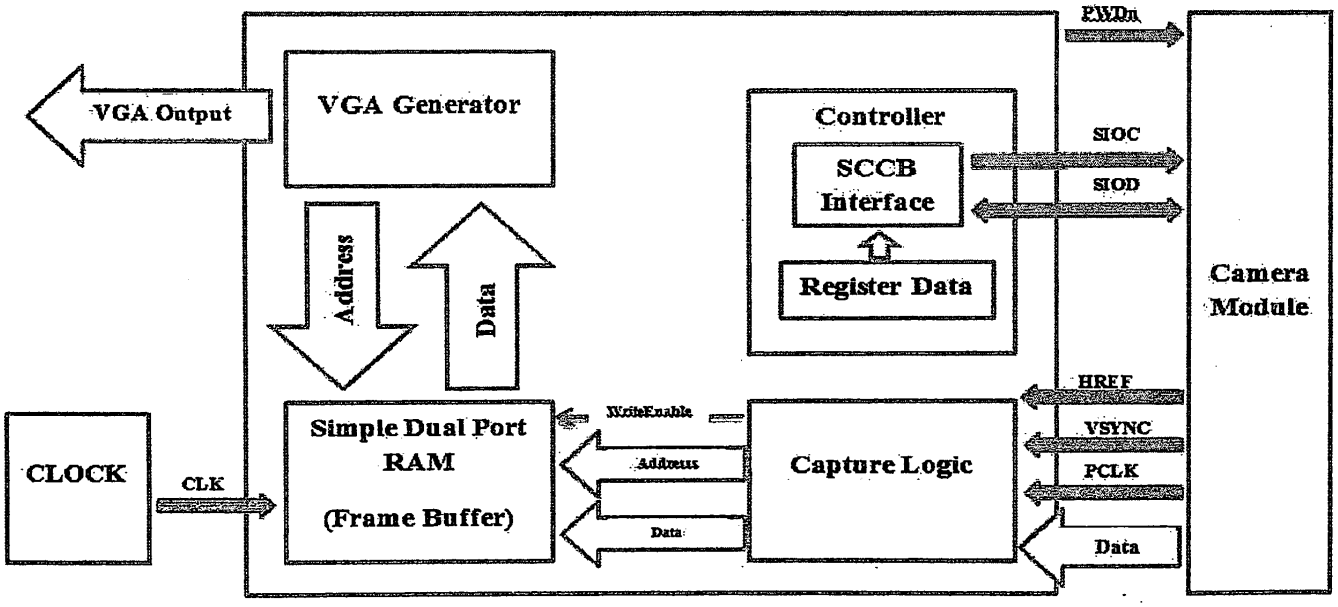

Figure 2: Block diagram of interfacing camera module with FPGA

The developed complete program loaded to the target device using USB Blaster device. Once the FPGA board is configured the Camera module starts capturing the real time video and displays it the VGA monitor interfaced with the FPGA board.For the storage purpose in this system uses Simple Dual Port RAM. It is capable with Read and Write function at a time. Therefore the system able captures each and every frame without missing. Due to this reason the output is really smooth. Following figure 3 shows the complete system.

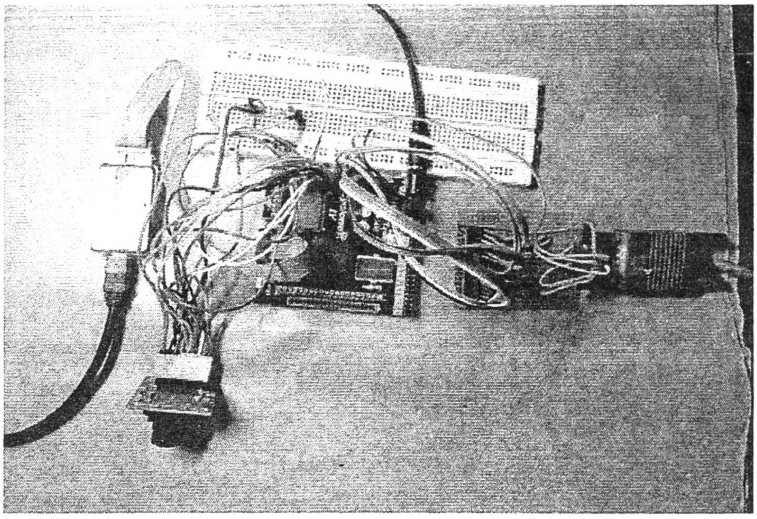

Figure 3: Complete system of the Hardware interface for camera module

3. RESULTS AND DISCUSSION

The design of the hardware interface for OV7670 is done in Verilog and VHDL. Design and testing of SCCB module has been carried out. The simulation result of OV7670 SCCB communication is shown in figure 4.

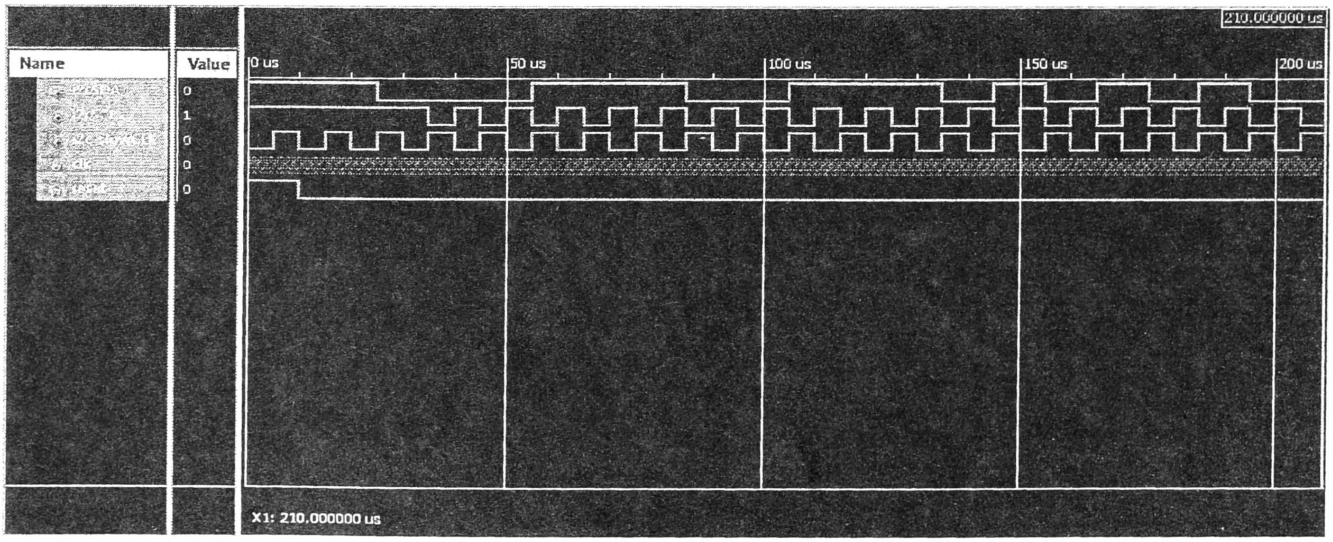

Figure 4: Simulation result of OV7670 SCCB module

The camera interface controller reads the 12 bit data from the camera module and storing in Simple dual port RAM. At the same time VGA controller reads the Simple dual port RAM and data were sent to the VGA monitor. Following figure 3 shows the result.

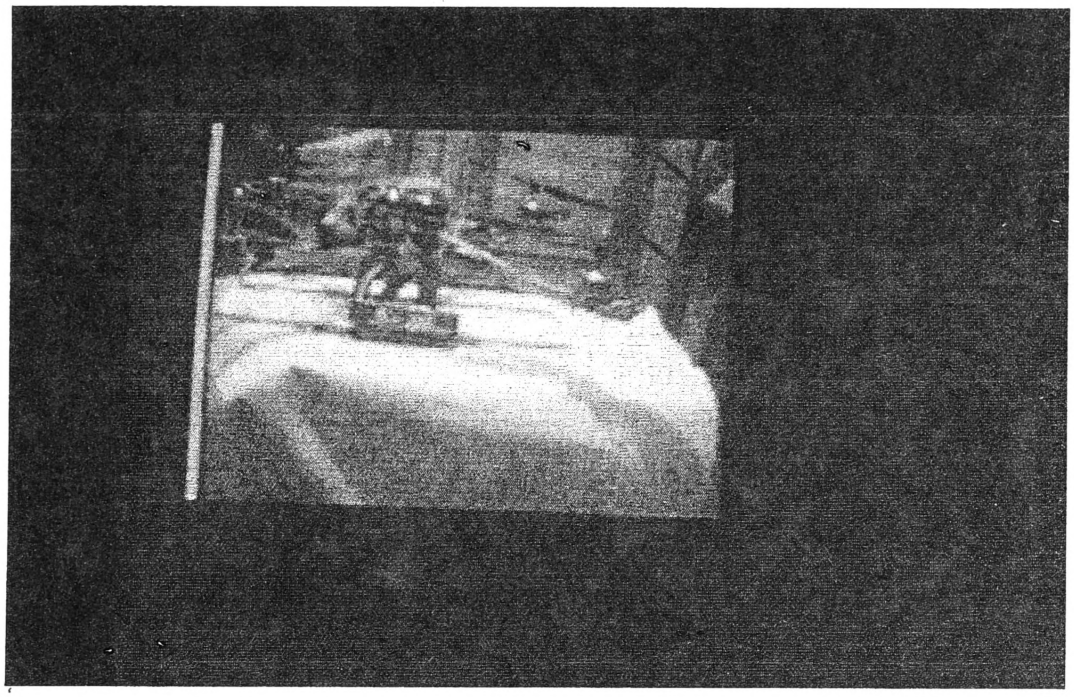

Figure 5: Final output of the complete system

Following Table 1shows the maximum resources that uses in FPGA for the complete system.

Table 1: Device utilization summary for project

Quartus II 32-bit Version	13.1.0 Build 162 10/23/2013 SJ Web Edition
Revision Name	camInterface
Top-level Entity Name	camInterface
Family	Cyclone IV E
Device	EP4CE15F17C8
Total logic elements	422 / 15,408 (3 %)
Total combinational functions	389 / 15,408 (3 %)
Dedicated logic registers	180 / 15,408 (1 %)
Total registers	180
Total pins	75 / 166 (45 %)
Total virtual pins	0
Total memory bits	236,544 / 516,096 (46 %)
Embedded Multiplier 9-bit	0 / 112 (0 %)

elements	
Total PLLs	1 / 4 (25 %)

The Table 1 shows the recourse utilization of the FPGA for the system. Synthesis of the designed camera interface reports, the total number of logic elements utilized by the design as 422(3%) with 180 registers (1%). Total number of pins configured with the inputs and outputs of the design as 75 from 166 pins with 236544 memory bits (46%) has been used and from total PLLs, only one is used. According to above table, the utilization of resources of FPGA is lower than 25% of its total capacity. Therefore, the rest of the logic resources of the FPGA could be used for video processing applications.

4. CONCLUSION

Real-time video processing is required in many applications such as industrial automation, machine vision systems, and robotics. FPGA logic resources can be used for implement high-speed, real-time video processing systems. As the first step, we demonstrated the design and implementation of a camera interface on an Altera Cyclone IV FPGA for OV7670 camera module. The results show that less amount of FPGA logic resources were consumed by the system and large amount of logic resources are available for implementing video processing algorithms in FPGA hardware. As an extension of this study, we intend to implement real-time edge detection algorithm for object inspection in industrial machine vision system.

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