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DDR MEMORY CONTROLLER FOR SPARTAN 3E FPGA

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ABSTRACT

Field Programmable Gate Arrays (FPGAs) are devices that can be configured to implement different types of digital systems. FPGAs come with large amount of logic resources, but they lack internal memory blocks. This limitation of internal memory blocks in FPGAs becomes a problem when memory-demanding systems are developed. As a solution to this problem external memory chips are integrated to the FPGA boards. For example, Spartan 3E Starter kit has a DDR SDRAM chip integrated to the FPGA board. Reading and writing operations of DDR memory is not straightforward. This paper describes the attempt to design a DDR memory controller for the Xilinx Spartan 3E FPGA to access the external memory.

Keywords: DDR SDRAM Controller, FPGA, Verilog

1. INTRODUCTION

A field-programmable gate array (FPGA) is an integrated circuit that consists of logic blocks of digital circuitry that can be programmed as hardware. Rather than being restricted to only certain hardware functions, as we are with application-specific Integrated circuits (ASICs), an FPGA can be programmed for specific functions and Applications[1]. As coprocessors, FPGAs have shown remarkable speedups for certain applications. The main reasons for achieving these performance gains come from the deep pipelines and parallel execution units that FPGAs have to offer[2].

For some applications FPGA's internal memory is not enough to gain high performance. But Spartan 3E starter kit board comes with the external memory and to get better performance we can combine that external memory with FPGA. From using Verilog Language an interface can be designed between FPGA and DDR SDRAM external memory. For the process of designing interface the users can use memory controller. The aim of this project is design a memory controller for the Spartan 3e FPGA.

Synchronous DRAM is the most suitable memory for this design because of its speed and pipelining capability[3]. In high-end applications, like microprocessors there will be specific built in peripherals to provide the interface to the SDRAM. But for other applications, the system designer must design a specific memory controller to provide command signals for memory refresh, read and write operation and initialization of SDRAM [4].

There are two types of SDRAM. They are single data rate SDRAM and Double Data Rate SDRAM. The Double Data Rate SDRAM read/write speed is better than Single Data Rate SDRAM. Because in Single Data Rate SDRAM's, data are transferred only at rising edge of the clock cycle and in Double Data Rate SDRAM's, data are transferred at both rising and falling edge of the clock cycle. Therefore the DDR SDRAM controllers are faster than Single Data Rate SDRAMs.

2. METHODOLOGY

The Spartan-3E Starter Kit boards include a 512 Mbit (32M x 16) Micron Technology DDR SDRAM (MT46V32M16) with a 16-bit data interface. All DDR SDRAM interface pins connect to the FPGA's I/O Bank 3 on the FPGA. I/O Bank 3 and the DDR SDRAM are both powered by 2.5V, and are generated by an LTC3412 regulator from the board's 5V supply input. The 1.25V reference voltage, common to the FPGA and DDR SDRAM, is generated using a resistor voltage divider from the 2.5V rail[5].

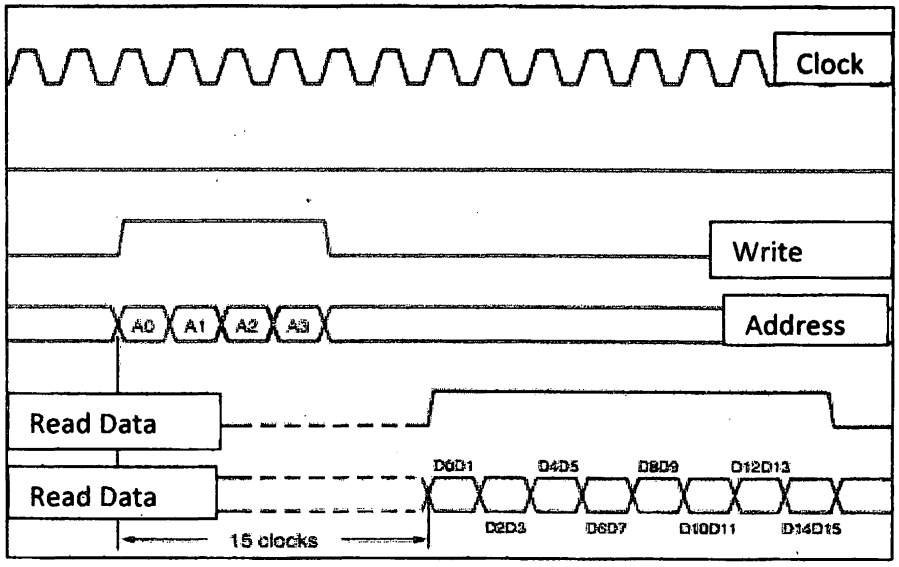

Figure 1: Timing diagram of the DDR SDRAM for read operation

Figure 1 shows the timing diagram for a user read burst. Read Data Valid and Read Data Out signals are user interface signals. Write-enable signal is for the reading of address and the Address signal is for the memory reading. The Read Data Valid signal is asserted when the

read data is available to the user, and Read Data Out is the read data from the memory to the user.

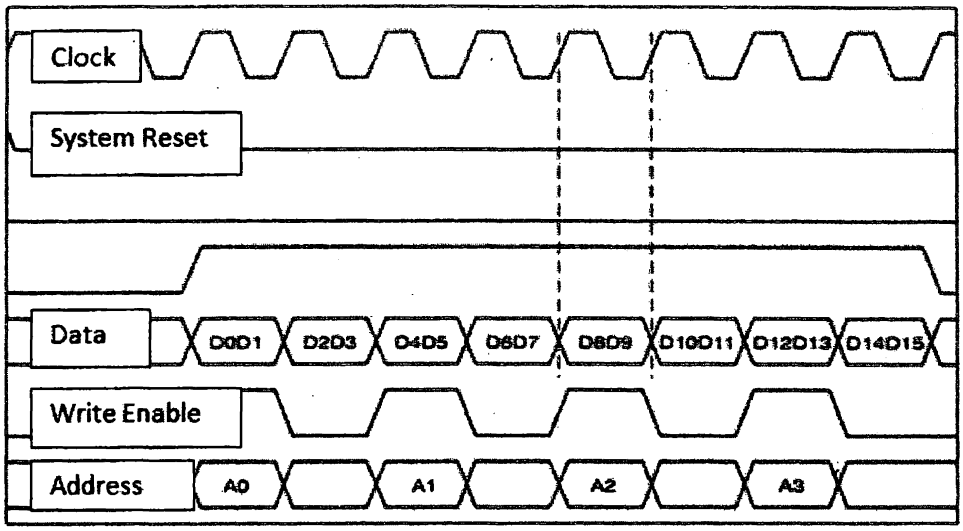

Figure 2: Timing diagram of the DDR SDRAM for write operation

Figure 2 shows the timing diagram for a user write burst. Write enable signal is to enable the writing process for the address and Address signal is for the identification of the correct location for the memory write. Data signal is used for writing the data to the memory. System Reset signal is used to reset the process.

Main Modules of DDR SDRAM

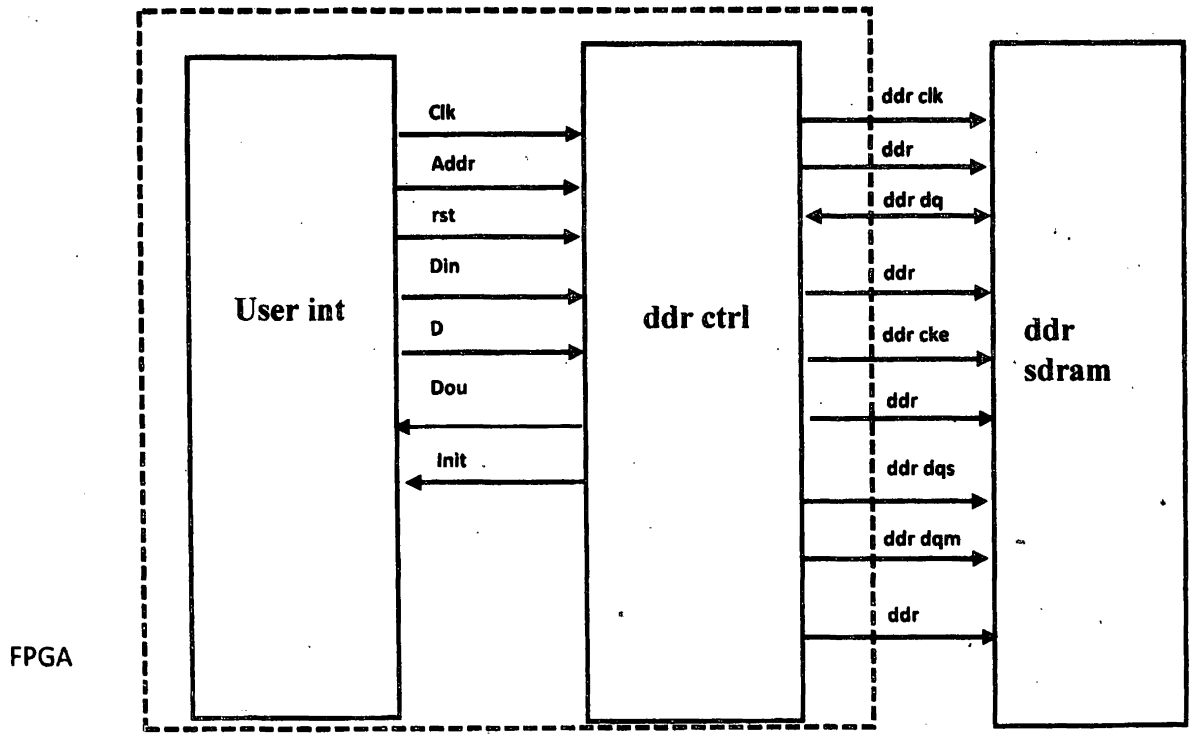

Figure 3: DDR SDRAM controller block diagram

ddr ctrl- The DDR SDRAM controller initializes the memory, accepts and decodes user commands, and generates READ, WRITE, and REFRESH commands. The DDR SDRAM controller also generates signals for other modules. The memory is initialized and is powered-up using a defined process. The controller state machine handles the initialization process upon power-up.

User int- This module stores write data in its Write Data FIFO (wr_data_fifo), write and read addresses in its Read/Write Address FIFO (rd_wr_addr_fifo), and receive read data from memory in its Read Data FIFO (rd_data_fifo). The width of the Write Data FIFO is twice the data width and mask width of the memory.

To create Interface between DDR SDRAM and FPGA, command signals should be used. Some of the command signals are shown below.

Main Command signals of the memory controller

Read -The READ command is used to initiate a burst read access to an active row.

Write-The WRITE command is used to initiate a burst write access to an active row.

Precharge -The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks.

NOP -The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform an NOP. This prevents unwanted commands from being registered during idle or wait states.

ACTIVE -The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access, like a read or write.

AUTO REFRESH -AUTO REFRESH is used during normal operation of the DDR SDRAM. This command is non persistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued[6].

3. RESULTS AND DISCUSSION

The design is simulated after combining the BUS master, DDR SDRAM controller and the DDR SDRAM[7]. The controller is designed using Verilog Hardware Description Language. For the design MT46V32M16 is chosen as DDR SDRAM. Results were observed from Isim

simulator. Below figure shows the results observed from the simulator. Spartan 3E starter kit board used to synthesis the results.

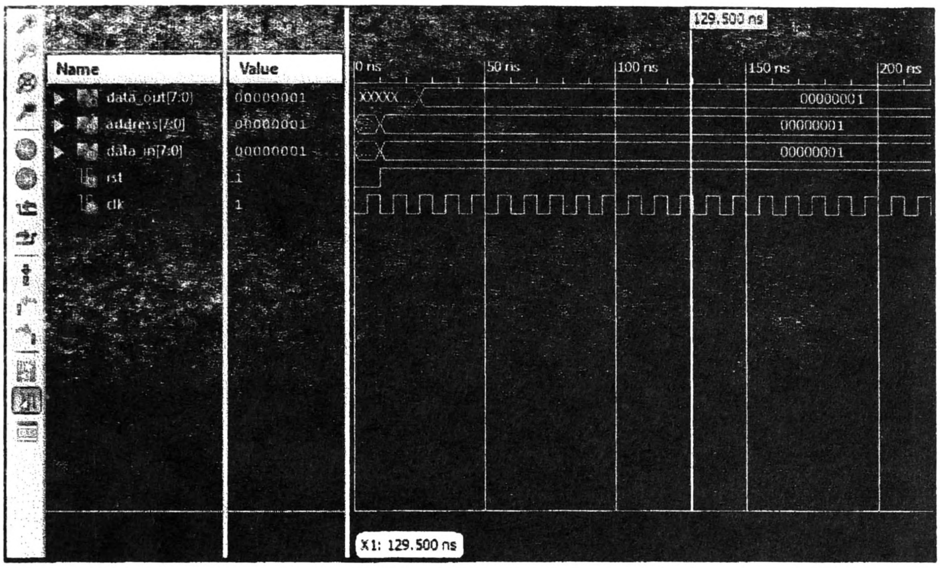

Figure 4: Read Write Process of simple memory

Above simulated results show the read write process of simple memory. Users' command is identified by the address [7:0]. Data Read Process is done from the address. Data write process shows by the data out [7:0] signal.

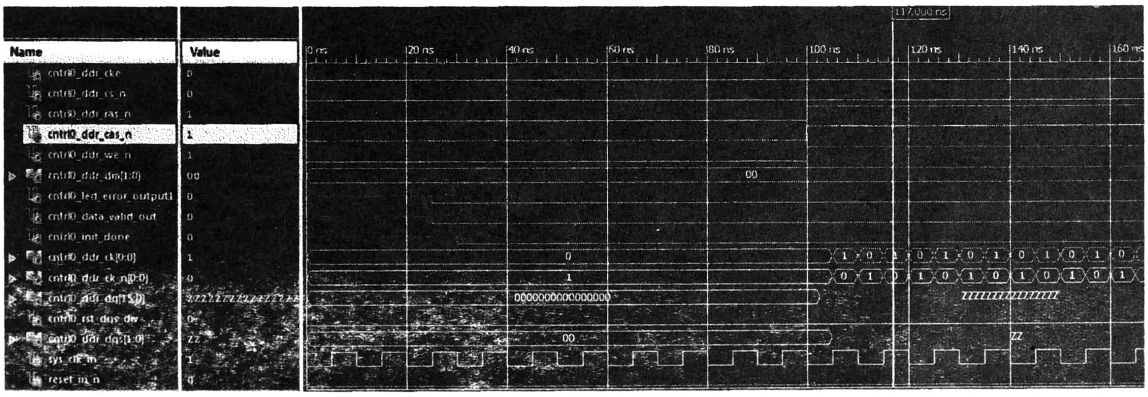

Figure 5: Memory controller output

There are two inputs which show above simulated diagram. Those are sys_clk_in and reset_in_n. Outputs are cntrl0_led_error_output, cntrl0_init_done and cntrl0_data_valid_out[7]. cntrl0_led_error_output performs high output when an error output occurs. cntrl0_init_done performs high output when the initialization process was done.

The advantages of DDR SDRAM memory controller are low power consumption and high transfer rate. Because of the property of general programmable interface it has replaced most of the parallel interface devices.

The application of DDR SDRAM is mostly in the real time devices due to its frequency of operation. In networking and communications applications large, fast memory devices are often required.

4. CONCLUSION

In this paper DDR SDRAM controller is designed and simulation results were obtained. The controller generates different types of timing and controlling signals, which synchronize the timing and controlling the flow of operation. The memory system operates at a double frequency rate of the processor, without affecting the performance. Thus we can reduce the data bus size. The drawback of this controller is complex schematic with large number of buffers in the circuit increases the amount of delay.

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