HARDWARE IMPLEMENTATION OF THE SOBEL EDGE DETECTION ALGORITHM

B.G. Jaykody and W.A.S. Wijesinghe

Department of Electronics, Faculty of Applied Sciences, Wayamba University of Sri Lanka, Kuliyapitiya, Sri Lanka

Corresponding author: susantha.wyb@gmail.com

Edge detection is a major operation in image processing applications. Most edge detection algorithms are implemented in software. Fast edge detection is required for real-time applications where software implementation of those algorithms may not suitable for such applications due to their slower processing power. This study proposes a hardware implementation of the Sobel edge detection algorithm. This algorithm computes the gradients in horizontal and vertical directions by using discrete differences of neighbouring pixels of an image. The magnitude of the sum of gradients is compared with a pre-defined threshold to determine whether there is an edge or not. Using Verilog hardware description language, this algorithm is ported into a Xilinx Spartan-3 Field Programmable Gate Array (FPGA). The Omni Vision OV7670 camera module generates 30 frames per second with the image resolution of 640×480 pixels. It continuously outputs 8-bit pixel data of image frames and the FPGA captures the data streams coming from the camera module. Once three lines of image data are buffered into the FPGA's Block RAM, the Sobel edge detection algorithm starts. The processed image data are sent to the VGA. The hardware algorithm is designed to store only three lines of image data at a time, which are sufficient to find the gradients in horizontal and vertical directions considering the four neighbouring pixels. This procedure avoids the need to store the complete image on the FPGA to compute the two gradients for edge detection. The hardware implementation of the Sobel edge detection algorithm shows significant speed performance over the software implementation of the algorithm using MATLAB. This technique can be used for machine vision systems in industrial applications such as real-time object inspection.

Keywords: FPGA, Real-time image processing, Sobel Edge Detection